Adaptive Clock Recovery (ACR)

Adaptive Clock Recovery is most commonly used for Circuit Emulation (CES). With CES a constant bit rate source stream is packetized and sent over the CEN. This data stream then has to be sent to the remote TDM equipment at exactly the same bit rate as it was emitted by the source. Even though both sides know the nominal rate (e.g. T1=1.544Mbps), the tolerance of the local oscillators can be ± a few parts per million. This means that over time the source can overrun the destination (if the source is faster) or underrun the destination (if the source is slower). Overruns and underruns cause quality problems with voice and video.

The problem can be seen in figure 1 at right. In the top part two PDH components are communicating directly. One device puts bits on the wire at a fixed rate and the receiving device (on the right in the diagram) can synchronize to the incoming bit stream. In the lower diagram a Carrier Ethernet Network is placed between the two devices and Circuit Emulation is used. Now there is no direct physical connection between the two PDH components. The bit stream is packetized on one side and de-packetized on the other. One function of the GIWF on the receiving end (right side in the diagram) is to put the bits on the wire at the exact rate that they came in on the other side of the CEN.

Adaptive Clock Recovery (ACR) is a method with several variants and implementations. In all of them, ACR reconstructs (recovers) the original clock for a synchronous data stream from the actual payload of the data stream. In other words, a synchronous clock is derived from an asynchronous packet stream.

The constant rate data stream is packetized at the source and sent through the CEN. These packets experience variable delay in the CEN. As long as the delay and the inter-frame delay variation are within reasonable bounds and the frame loss ratio is very low, the receiving GIWF can maintain an average receive rate for the CES packets and use that rate to adjust the transmit clock for the TDM bit stream. The algorithms are fairly complex since adjustments of the clock have to be made in very small increments and very infrequently in order to meet the jitter and wander requirements of the various PDH standards.

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